Modified Stanford-PKU RRAM model to simulate multilevel SET process in 1T1R arrays.

If you have benefited from this model, please refer to the following paper and cite it:

John Reuben, Dietmar Fey and Christian Wenger, "**A modeling methodology for Resistive RAM based on Stanford-PKU model with extended multilevel capability**", IEEE Transactions on Nanotechnology, 2019

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Multilevel Modeling using Stanford RRAM model

In RRAMs, there are two ways to implement multiple states

1) By varying compliance current (also called multilevel SET): from the initial HRS, the RRAM is programmed to different LRS during the SET process

2) By varying reset voltage (also called multilevel RESET): from the initial LRS, the RRAM is programmed to different HRS during the RESET process

Since HRS variability is more compared to LRS variability in RRAM arrays, we prefer multilevel- SET process. I.e single HRS and multiple LRS. Multilevel SET is demonstrated in 1T1R arrays by IHP and other research groups.

SET, RESET and READ process in 1T-1R

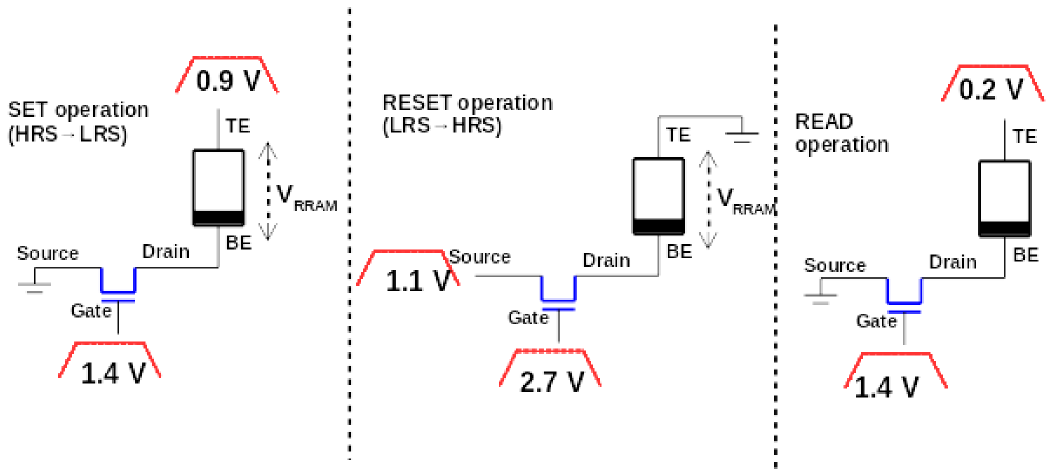

Fig.2 : Voltage pulses during SET, RESET and READ process. (The duration of SET and RESET pulses is 10 µS)

IHP's 1T-1R charactersitcs

Important observation: Read-out voltage is 0.2 V

So the characteristic of IHP's RRAM are as follows:

HRS= 66.66 KΩ (3µA at 0.2 V)

LRS1= 10 KΩ (20µA at 0.2 V) when gate voltage is 1.2 V

LRS2 = 6.66 KΩ (30µA at 0.2 V) when gate voltage is 1.4 V

LRS3= 5 KΩ (40µA at 0.2 V) when gate voltage is 1.6 V

Composite 1T1R model

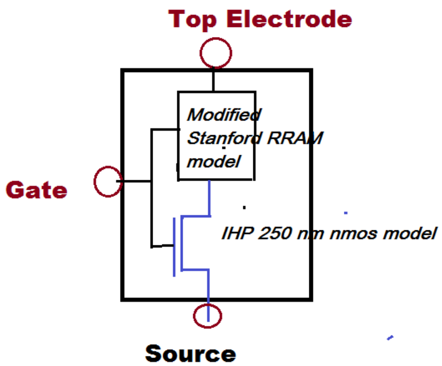

Fig. 1

Modified Stanford RRAM model (Verilog-A code)

```
`include "constants.vams"
`include "disciplines.vams"

module Stanford_modified(TE, BE, vgate);
input vgate;
inout                    TE, BE;
electrical          TE, BE;
electrical vgate;
//  Version Parameter
parameter real               version               = 1.00 from(0:inf);
// Switch to select Standard Model (0) or Dynamic Model (1)
parameter integer      model_switch                = 0    from[0:1];

//  The following constants have been pre-defined in the constants.vams
//  Boltzmann's constant in joules/kelvin, 'parameter real kb =  1.3806503e-23'
parameter real               kb =  1.3806503e-23;
//  charge of electron in coulombs, 'parameter real q =  1.6e-19'
parameter real               q                     =  1.6e-19;
  //  average switching fitting parameters g0, V0, I0, beta, gamma0
parameter real               g0                    = 0.25e-9 from(0:2e-9);
parameter real               V0                    = 0.25    from(0:10);
parameter real               Vel0                  = 10    from(0:1000);
parameter real               I0                    = 1000e-6 ;// from(0:1e-2);
parameter real               beta                  = 0.8    from(0:inf);
parameter real               gamma0                = 16  from(0:inf);
//  threshold temperature for significant random variations
parameter real               T_crit                = 450               from(390:460);
//  variations fitting parameters
parameter real        deltaGap0  = 0.02            from[0:0.1);

parameter real               T_smth                = 500               from(400:600);//  activation energy for vacancy generation
parameter real               Ea                    = 0.6 from(0:2);
//  atom spacing, a0
parameter real               a0                    = 0.25e-9 from(0:inf);
```

```
//  initial room temperature in devices
parameter real                    T_ini                 = 273 + 25 from(0:inf);
//  minimum field requirement to enhance gap formation, F_min
parameter real                    F_min                 = 1.4e9 from(0:3e9);
// For IHP's transistor, W/L=1140/240 which is 4.75
parameter real W_by_L = 4.75;
//  initial gap distance, gap_ini
parameter real                    gap_ini               = 2e-10 from(0:100e-10);
//  minimum gap distance, gap_min
// This is the main modification:g_min is a function of gate voltage and W/L of transistor
real gap_min;
//  maximum gap distance, gap_max


parameter real                    gap_max               = 19e-10 from(0:100e-10);
//  thermal resistance
parameter real                    Rth                   = 1.5e3 from(0:inf);
//  oxide thickness, thickness
parameter real                    tox                   = 12e-9 from(0:100e-9);
// initial random seed
parameter integer      rand_seed_ini          = 0 from(-1.6e9:1.6e9);
// time step boundary
parameter real                    time_step  = 3e-9 from(1e-15:1);
//  voltage V(TE, BE), Vtb; current I(TE, BE), Itb
real                              Vtb, Itb;
// Voltage at Gate of transistor;
real Vg;
//  present temperature in devices, temp
real                              T_cur;
//  gap time derivative, gap_ddt; random gap time derivative, gap_random_ddt
real                              gap_ddt, gap_random_ddt;
//  present gap status
real                              gap;
//  local enhancement factor, gamma
real                              gamma;
real                              gamma_ini;
//  random number
integer                           rand_seed;
real                              deltaGap;


parameter real                    pulse_width = 20n;
              analog begin
// bound time step
                         $bound_step(time_step);
// present Vtb, Itb, and local device temperation calculation, T_cur
                         Vtb = V(TE,BE);
                         Itb = I(TE,BE);
      Vg=V(vgate);
                         T_cur = T_ini + abs( Vtb * Itb * Rth);
// calculate g_min

  gap_min = (2.6e-10 * ( W_by_L / Vg)) + 1.21e-10;//previously 2.6e-10.....+ 1.21e-10

//$display("voltage across RRAM is  =%e",Vtb):
//  gap_min              = (2.6e-10 * ( W_by_L / (Vg-0.9+((Vtb/0.3)/sqrt((1+pow((Vtb/0.3),2))))))) + 1.21e-10;
//$display("Value of gap_min = %e ", gap_min);
// initialize random seed, rand_seed
                         @(initial_step)
                                      rand_seed = rand_seed_ini;

// calculate local enhancement factor, reference RRAM_CompactModel_I.pdf
// added
                         gamma_ini = gamma0;
```

```
//added
			if(Vtb < 0) begin
				gamma_ini = 16;
			end
			gamma = gamma_ini - beta * pow((( gap )/1e-9), 3);

			if ((gamma * abs( Vtb )/ tox) < F_min) begin
				gamma = 0;
			end

// calculate next time step gap situation
// gap time derivative - determinant part
			gap_ddt = - Vel0 * exp(- q * Ea / kb / T_cur) * sinh(gamma * a0 / tox * q * Vtb / kb / T_cur);
// gap time derivative - variation part
			deltaGap = deltaGap0 * model_switch;
			gap_random_ddt = $rdist_normal(rand_seed, 0, 1) * deltaGap / (1 + exp((T_crit - T_cur)/T_smth));
			gap = idt(gap_ddt+gap_random_ddt, gap_ini);
	//		if(gap<gap_min) begin
	//			gap =  gap_min;
	//		end else if ( gap>gap_max) begin
	//			gap=gap_max;
//			end
    if ( gap>gap_max) begin
				gap=gap_max;
			end
			Itb = I0 * exp(-gap/g0)*sinh(Vtb/V0);
			I(TE,BE)<+Itb;
			end
endmodule
```

Characteristics of IHP's 1T1R

HRS= 66.66 KΩ (3μA at 0.2 V)

LRS1= 10 KΩ (20μA at 0.2 V) when gate voltage is 1.2 V

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LRS3= 5 KΩ (40μA at 0.2 V) when gate voltage is 1.6 V

Parameters of modified Stanford RRAM model

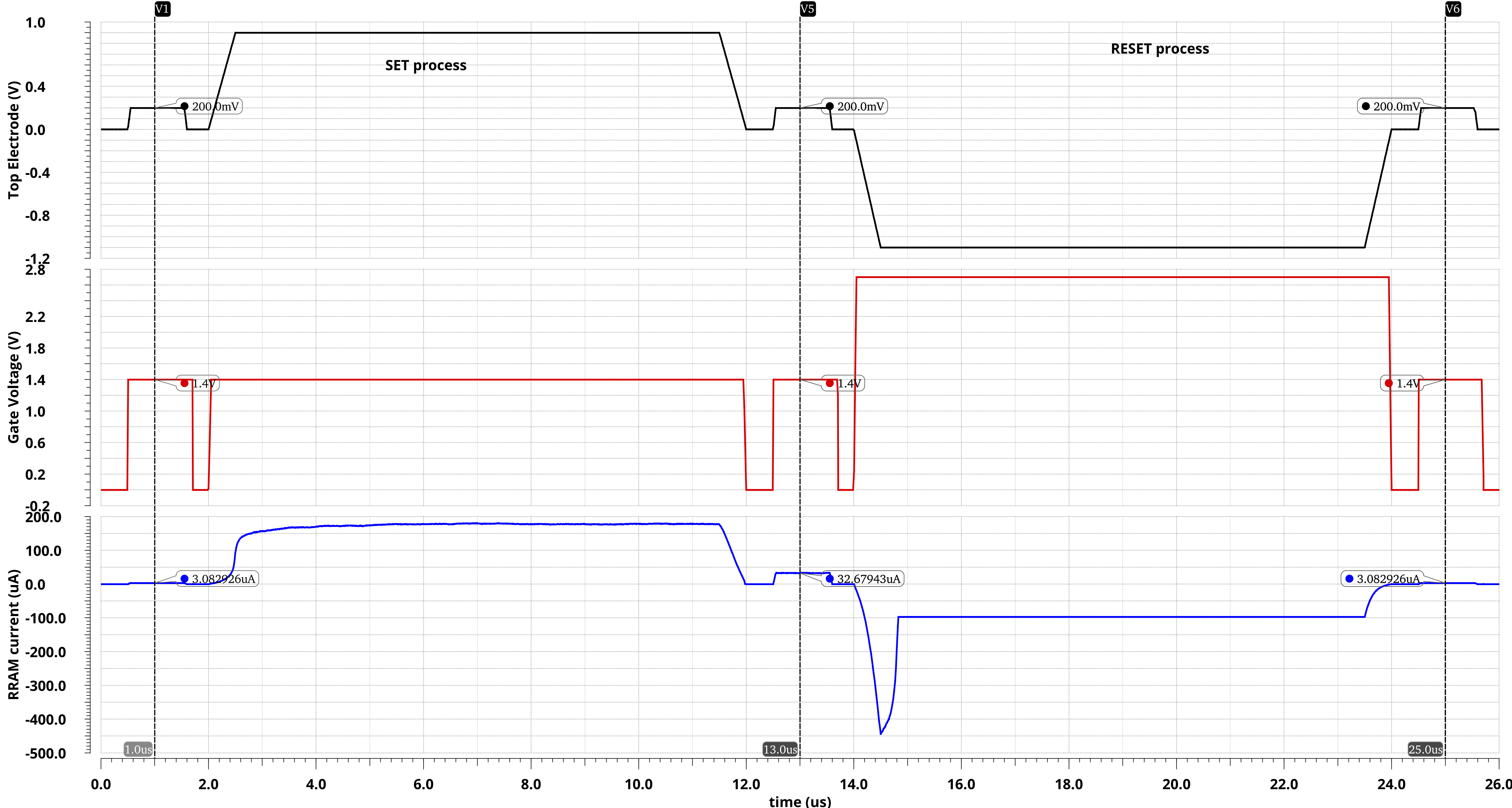
Ea=0.6	I0=8.54e-4	Rth=1500	model_switch=1	g0=0.346e-9	V0=0.26	Vel0=0.05
Beta=0.4	gamma0=19.5	T_crit=450	DeltaGap0=0.005	T_smth=500	a0=2.5e-10	Tini=298
F_{min}=1.4e9	gap_ini=18.8e-10		gap_max=18.8e-10	tox=6e-9	Time_step=1e-9	

NMOS model parameters:

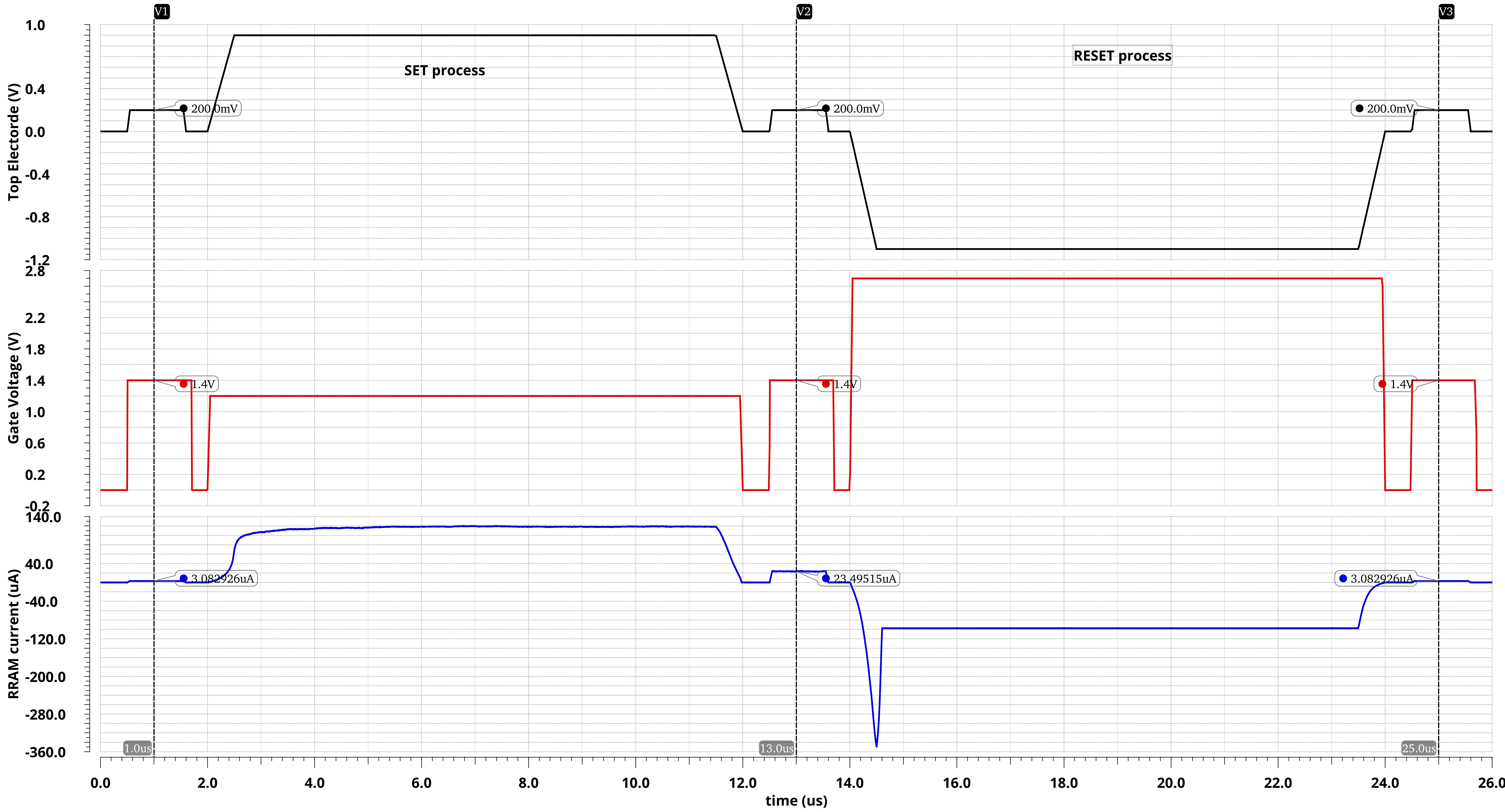
t_{ox} = 10 nm, W = 1.14 m, L = 0.24 m, V_t (threshold voltage of MOSFET)= 0.6 V

Simulation Steps:

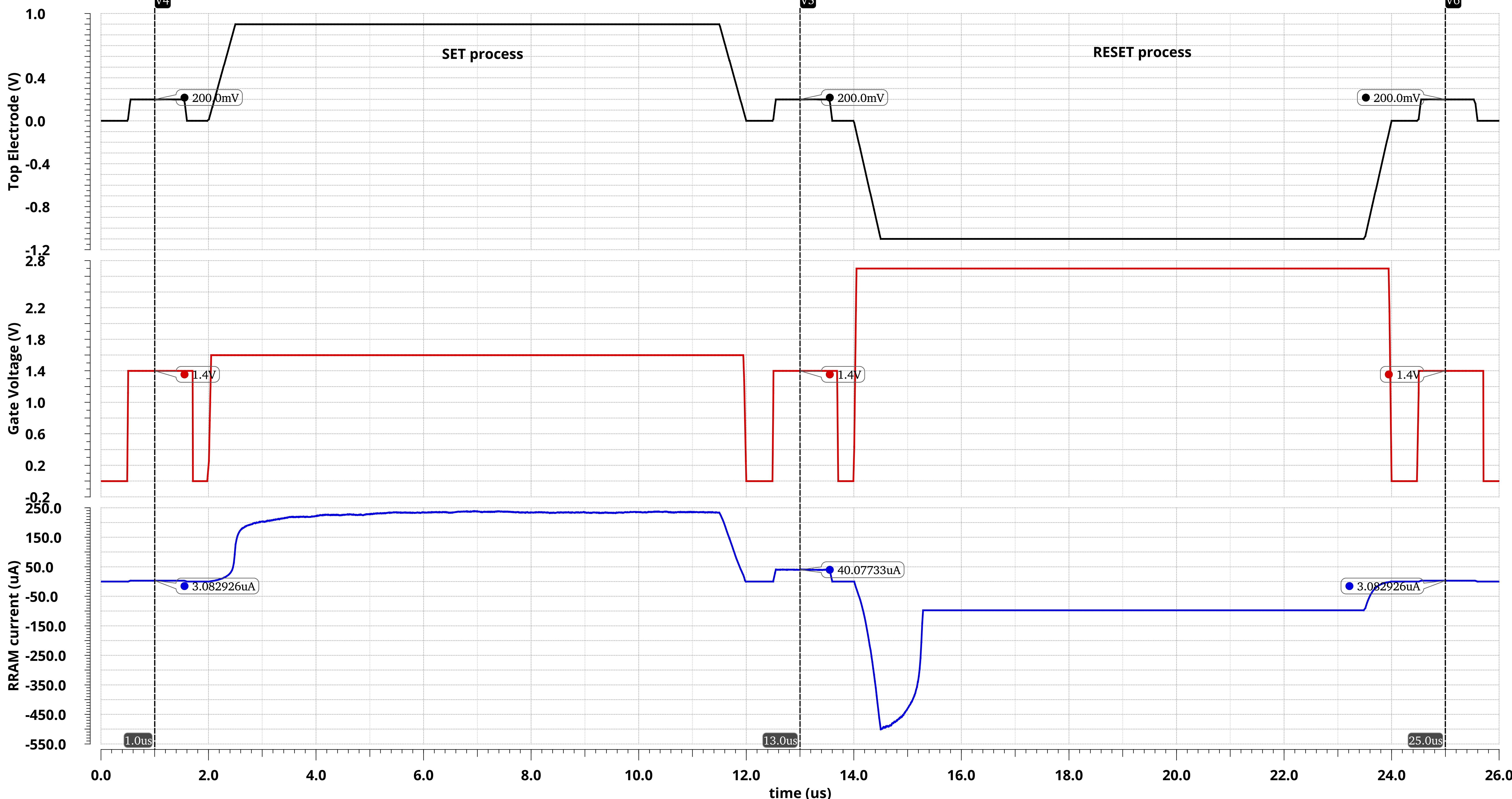
1. Create a RRAM model by instantiating "Modified Stanford RRAM model" verilog-A code
2. Create nmos transistor by instantiating "nmos" from SGB25_dev (IHP's 250 nm CMOs library files must be installed already in the Cadence Virtuoso environment)
3. Create composite 1T1R model as shown in Fig.1
4. Set gap_ini= 18.8e-10 and simulate SET process with voltage pulses as illustrated in Fig.2. Sample wave forms of the multilevel SET process is plotted in Figure below
5. Set gap_ini= 18.8e-10 and simulate SET process followed by RESET to verify if the RRAM returns to the same HRS of 3 μA in each case.



V1
V5
V6
SET process
RESET process
Top Electrode (V)
Gate Voltage (V)
RRAM current (uA)
time (us)
200.0mV
1.4V
3.082926uA
32.67943uA
1.0us
13.0us
25.0us



V1
V2
V3
SET process
RESET process
Top Electorde (V)
Gate Voltage (V)
RRAM current (uA)
200.0mV
1.4V
3.082926uA
23.49515uA
1.0us
13.0us
25.0us
time (us)



SET process
RESET process
Top Electrode (V)
Gate Voltage (V)
RRAM current (uA)
time (us)
200.0mV
1.4V
3.082926uA
40.07733uA
1.0us
13.0us
25.0us