FARHAD EBRAHIMI

Digital Design Engineer | RISC-V & SoC | FPGA & ASIC

Germany | Email | Homepage | Linkedin | GitHub

EXPERIENCE

Hardware Design Engineer

FAU Erlangen-Nürnberg

Apr 2022 – Present — Erlangen, Germany

- Designed and implemented a custom **RISC-V core (RTL)** with custom ISA extensions
- Developed and integrated complete **SoC designs**, including a memory subsystem with a custom bus interface and Wishbone-connected peripherals (UART, TIMER, GPIO)
- Implemented, verified, and deployed designs on **Zynq-7000 and Zynq UltraScale+ FPGA** platforms
- Initiated **PetaLinux** with an Ubuntu rootfs on the UltraScale+ family and developed drivers to interface with PL IP cores
- Established an **RTL-to-ASIC open-source design flow** targeting the IHP 130 nm open PDK

Lecturer

FAU Erlangen-Nürnberg

Oct 2022 – Present — Erlangen, Germany

- Delivered graduate-level lectures on **supercomputer architecture**
- Supervised M.Sc. and B.Sc. theses in **hardware design and RISC-V**

SELECTED PROJECTS

- **NOVACore – RISC-V Processor and SoC**
  Designed a 7-stage in-order RISC-V CPU with CSD-driven arithmetic and custom ISA extensions. Performed RTL design, verification, and FPGA implementation on Zynq-7000 and UltraScale+ platforms.
- **RTL-to-Silicon Open-Source ASIC Flow**
  Developed an end-to-end ASIC design flow for NOVACore targeting the IHP 130 nm open PDK, from RTL to GDS-ready stages.
- **Custom SoC Design on FPGA**
  Designed and implemented a complete SoC including the NOVACore CPU, FSBL/SSBL, main memory, and Wishbone-connected UART and TIMER peripherals.
- **Hardware Accelerators**
  Designed a systolic array for FPGA-based matrix multiplication acceleration using AXI DMA in interrupt-based direct register mode.

PUBLICATIONS

- **F. Ebrahimiazandaryani**, et al., "Silicon-Based Evaluation of CSD Arithmetic in a RISC-V Processor Using Open-Source ASIC Flow," *IEEE ISCAS*, 2026.
- **F. Ebrahimi-Azandaryani**, et al., "CSD-Driven Speedup in RISC-V Processors," *DASIP | HiPEAC*, 2025.
- **F. Ebrahimi-Azandaryani**, et al., "Extern: Boosting RISC-V Core Performance using Ternary Encoding," *Microprocessors and Microsystems*, 2024.

Google Scholar

ABOUT ME

Hardware and Digital Design Engineer with 4+ years of hands-on experience in CPU(RISC-V) and SoC development, spanning RTL design, FPGA prototyping, and ASIC-oriented flows. I enjoy working on complex hardware systems and translating architectural concepts into efficient, implementable designs. Outside of work, I maintain an active lifestyle through the gym and have a strong interest in classical music.

EDUCATION

M.S. in Computer Science

University of Tehran

Sept 2016 – Feb 2019

TOOLS & SKILLS

Hardware Design: VHDL, Verilog, Tcl, cocotb
EDA Tools: Vivado, ModelSim, Yosys, GHDL
Embedded & Programming: PetaLinux, C/C++, OpenMP, CUDA
Workflow: Git (GitHub, GitLab)

FIELDS OF EXPERTISE

Computer Architecture | CPU & RISC-V | HW Accelerator | Computer Arithmetic | Approximate computing | Digital Design | ASIC/FPGA | Re-configurable computing

LANGUAGES

German	Basic (A2–B1)
English	Professional (B2–C1)
Azerbaijani	Native
Persian	Native

REFEREES

Prof. Dietmar Fey
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Prof. Ali Afzali Kusha
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